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EXAMINER	
STEVENS, THOMAS H	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,933	WU ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-20,22-39,52-58,61-65,76,77 and 91-98* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-20,22-39,52-58,61-65,76,77 and 91-98* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/05 & 10/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7,9-20,22-39,52-58,61-65,76-77,91-98 examined.

2. Claims 8,21,40-51,59-60,66-75,78-90 were canceled.

Claim Objections

3. Claims 91 is objected to by which this apparatus dependent claim is linked to a independent and dependent method claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1-7,9-20,22-39,52-58,61-65,76-77,91-98 are rejected under 35 U.S.C. 102(b) as being disclosed by Jiang et al. ("Key Hot-Carrier Degradation (pg. 300, Introduction) Model Calibration and Verification Issues for Accurate AC Circuit-Level Reliability Simulation" IEEE 1997) (hereafter Jiang). Jiang discloses a degradation (pg. 300, Introduction) model study for alternating current circuits (abstract).

Claim 1. A method of simulating the degradation (pg. 300, Introduction) of a circuit, comprising: providing a netlist (inherent to SPICE program, pg. 300, Introduction)

specifying the components of the circuit; supplying a plurality of circuit stress (pg. 300, right column lines 10-11) time values (pg. 305, right column, 2nd paragraph); supplying aging model information on selected ones of the components; simulating the behavior of the fresh circuit to determine for each of the selected components a component degradation (pg. 300, Introduction) parameter relative to circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph); and determining the degradation (pg. 300, Introduction) parameter relative to circuit by simulating the operation of the circuit with the specified components using their respective aging model information and respective relative component degradation (pg. 300, Introduction) parameter at the supplied circuit stress (pg. 300, right column lines 10-11) time values (pg. 305, right column, 2nd paragraph).

Claim 2. The method of claim 1, wherein said degradation (pg. 300, Introduction) of the circuit is due to hot-carrier effects (title).

Claim 3. The method of claim 1, wherein the simulating is performed using a SPICE type circuit simulator (pg. 300, abstract and "Summary of existing model).

Claim 4. The method of claim 1, wherein the simulating is performed using a timing simulation type circuit simulator (pg. 300, abstract and "Summary of existing model).

Claim 5. The method of claim 1, wherein the aging model information on the selected ones of the components is derived from electrical test data (inherent to SPICE program, pg. 300, Introduction).

Claim 6. The method of claim 1, wherein said simulating the behavior of the fresh circuit determines the waveforms at the nodes (pg. 304, left column, last paragraph) to which the selected ones of
the components are connected relative to an input waveforms (pg. 304, left column, last paragraph).

Claim 7. The method of claim 1, wherein determining the degraded operation of the circuit comprises determining the circuit's speed (specification pg. 8, last 2 sentence disclose the speed or delay of current drain; thus results are compared to benchmark: pg. 300, introduction last 9 lines with figure 11 pg.305) at the supplied circuit age parameters.

Claim 9. The method of claim 93, wherein the distinct sets of components each form different functional blocks (specification, pg 6, line 3 defines functional blocks "analog to digital sector", thus pg. 300, left column, last 9 sentences).

Claim 10. The method of claim 8, wherein a first of said sets of components is an analog block and a second of said sets of components is a digital block (specification,

pg 6, line 3 defines functional blocks "analog to digital sector", thus pg. 300, left column, last 9 sentences).

Claim 11. The method of claim 10, wherein the performance criterion of the first set is transconductance and the performance criterion of the second set is drain (design choice, see In re Stevens) to source current (pg. 302, Evaluating Degradation Model Precision section).

Claim 12. The method of claim 8, wherein the distinct sets of components consist of different device types (pg. 304, right column, AC Degradation Model Validation section, comparison).

Claim 13. The method of claim 12, wherein a first of said different device types is an NMOS and a second of said different device types is a PMOS (pg. 304, left column, last paragraph).

Claim 14. The method of claim 13, wherein the PMOS (pg. 304, left column, last paragraph)performance criterion is leakage current (reverse bias of a transistor thus inherent).

Claim 15. The method of claim 13, wherein the NMOS (pg. 304, right column, 1st paragraph) performance criterion is driving capability.

Claim 16. The method of claim 12, wherein a first of said different device types is a MOSFET (pg. 301, left column, 3rd paragraph)and a second of said different device types is a bipolar junction
transistor.

Claim 17. The method of claim 16, wherein the bipolar junction transistor performance criterion is leakage current (reverse bias of a transistor thus inherent).

Claim 18. The method of claim 93, wherein the distinct sets of components employ different models for simulating the same device type (pg. 304, right column, AC Degradation Model Validation section, comparison).

Claim 19. The method of claim 93, wherein the distinct sets of components consist of the same device type (pg. 304, right column, AC Degradation Model Validation section, comparison).

Claim 20.The method of claim 93, wherein the distinct sets of components form functional blocks (specification, pg 6, line 3 defines functional blocks “analog to digital sector”, thus pg. 300, left column, last 9 sentences)column, 2nd paragraph) performing the same function.

Claim 22. The method of claim 94, wherein the first and second sets of components each form different functional blocks (specification, pg 6, line 3 defines functional blocks "analog to digital sector", thus pg. 300, left column, last 9 sentences).

Claim 23. The method of claim 94, wherein the second set components form a digital block (specification, pg 6, line 3 defines functional blocks "analog to digital sector", thus pg. 300, left column, last 9 sentences).

Claim 24. The method of claim 23, wherein the specified degradation (pg. 300, Introduction) level is expressed in terms of drain (simulating drain current: pg.303, right column) to source current degradation (pg. 300, Introduction).

Claim 25. The method of claim 94, wherein the second set of components is an analog block (specification, pg 6, line 3 defines functional blocks "analog to digital sector", thus pg. 300, left column, last 9 sentences).

Claim 26. The method of claim 25, wherein the specified degradation (pg. 300, Introduction) level is expressed in terms transconductance degradation (pg. 300, Introduction).

Claim 27. The method of claim 94, wherein the first and second sets of components each consist of different device types (analog and digital devices, pg. 300, left column, last 9 lines).

Claim 28. The method of claim 27, wherein the second set of components consists of PMOS transistors (pg. 301, left column, 1st paragraph).

Claim 29. The method of claim 28, wherein the specified degradation (pg. 300, Introduction) level is expressed in terms of leakage current (reverse bias of a transistor thus inherent) degradation (pg. 300, Introduction).

Claim 30. The method of claim 27, wherein the second set of components consists of NMOS transistors (pg. 304, right column, 1st paragraph).

Claim 31. The method of claim 30, wherein the specified degradation (pg. 300, Introduction) level is expressed in terms of driving capability degradation (pg. 300, Introduction).

Claim 32. The method of claim 27, wherein the second set of components consists of bipolar junction transistors (inherent to the property of transistors: pg. 304, right column, 1st paragraph).

Claim 33. The method of claim 32, wherein the specified degradation (pg. 300, Introduction) level is expressed in terms of leakages current degradation (pg. 300, Introduction).

Claim 34. The method of claim 94, wherein the first and second sets of components employ different models for simulating the same device type (pg. 304, right column, AC Degradation Model Validation section, comparison).

Claim 35. The method of claim 94, wherein the first and second sets of components each consist of the same device type (pg. 304, right column, AC Degradation Model Validation section, comparison).

Claim 36. The method of claim 94, wherein the first and second sets of components form functional blocks (specification, pg 6, line 3 defines functional blocks "analog to digital sector", thus pg. 300, left column, last 9 sentences)column, 2nd paragraph) performing the same function.

Claim 37. The method of claim 94, wherein the degradation (pg. 300, Introduction) level of the second set of selected components is specified as a relative component degradation (pg. 300, Introduction) parameter with respect to the component degradation (pg. 300, Introduction) parameter of the first set of components.

Claim 38. The method of claim 94, wherein the degradation (pg. 300, Introduction) level of the second set of selected components is expressed in terms of age (pg. 303, right column, 1st paragraph).

Claim 39. The method of claim 94, wherein the degradation (pg. 300, Introduction) level of the second set of selected components is expressed in terms of lifetime (pg. 305, right column, 2nd paragraph) (pg. 303, right column, 1st paragraph).

Claim 52. The method of claim 95, wherein the selected components are MOSFETs (pg. 301, left column, 3rd paragraph).

Claim 53. The method of claim 95, wherein said degradation (pg. 300, Introduction) of the circuit is due to hot carrier effects (title).

Claim 54. The method of claim 52, wherein for each of said selected components more than one of said plurality of independent current sources (pg. 302, right column, Evaluating Degradation Model Precision) are connected between the source and drain (simulating drain current: pg.303, right column) terminals of the non-aged version (pg. 304, right column, AC Degradation Model Validation).

Claim 55. The method of claim 52, wherein said method further includes: determining the magnitude of the respective current in each of the independent current sources (pg. 302, right column, Evaluating Degradation Model Precision), said determining comprising: supplying a physical model of the current magnitude; and establishing the

values of the coefficients (pg. 300, right column, Summary of Existing Model, acceleration coefficient) in the physical model from electrical test data.

Claim 56. The method of claim 52, wherein the degradation (pg. 300, Introduction) level of the selected components is expressed in terms of lifetime (pg. 305, right column, 2nd paragraph) (pg. 303, right column, 1st paragraph).

Claim 57. The method of claim 52, wherein the degradation (pg. 300, Introduction) level of the selected components is expressed in terms of age.

Clam 58. The method of claim 95, wherein said simulating the operation of the circuit is performed with a circuit simulator (pg. 300, abstract and "Summary of existing model) and wherein said revising the netlist (inherent to SPICE program, pg. 300, Introduction) is embedded in the circuit simulator (pg. 300, abstract and "Summary of existing model).

Claim 61. The method of claim 97, wherein the selected components are MOSFETs (pg. 301, left column, 3rd paragraph) and said incorporating the aging of the selected components comprises including the time (pg. 305, right column, 2nd paragraph) dependence of the drain (simulating drain current: pg.303, right column) to source current.

Claim 62. The method of claim 61, wherein said incorporating the aging of the selected components comprises including the time (pg. 305, right column, 2nd paragraph) dependence of the substrate current.

Claim 63. The method of claim 61, wherein said incorporating the aging of the selected components comprises including the time (pg. 305, right column, 2nd paragraph) dependence of the gate current.

Claim 64. The method of claim 97, wherein said simulating the behavior of the circuit to determine for each of the selected components a component degradation (pg. 300, Introduction) parameter relative to circuit age comprises: simulating the behavior of the fresh circuit to determine for each of the selected components an intermediate component degradation (pg. 300, Introduction) parameter relative to circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph); determining the degraded operation of the circuit at an intermediate circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) value by simulating the operation of the circuit with each of the specified components using the respective aging model information and respective relative intermediate component degradation (pg. 300, Introduction) parameter at the intermediate circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) value; and simulating the behavior of the degraded circuit at the intermediate circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) value to determine for each of

the selected components a component degradation (pg. 300, Introduction) parameter relative to circuit age, wherein the intermediate circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) value is less than one of the circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) values.

Claim 65. The method of claim 97, wherein said simulating the operation of the circuit is performed with a circuit simulator (pg. 300, abstract and "Summary of existing model) and wherein said incorporating the aging of the selected components by updating the modules of said circuit simulator (pg. 300, abstract and "Summary of existing model) is embedded in the circuit simulator (pg. 300, abstract and "Summary of existing model).

Claim 76. The method of claim 98, wherein said determining comprises: revising the netlist (inherent to SPICE program, pg. 300, Introduction), wherein each of said selected components is replaced by a non-aged version of the selected component and a plurality of independent current sources (pg. 302, right column, Evaluating Degradation Model Precision) corresponding to different mechanisms with distinct quantized relative degradation (pg. 300, Introduction) level connected between the terminals of the non-aged version, the magnitude of the respective quantized current in each of the current sources (pg. 302, right column, Evaluating Degradation Model Precision) determined from the aging model information of component; and determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist

(inherent to SPICE program, pg. 300, Introduction), the independent current magnitudes derived form the respective aging model information and respective relative degradation (pg. 300, Introduction) level at the supplied circuit stress (pg. 300, right column lines 10-11) time value (pg. 305, right column, 2nd paragraph).

Claim 77. The method of claim 98, wherein said simulating the operation of the circuit is performed with a circuit simulator (pg. 300, abstract and "Summary of existing model) and wherein said quantizing is embedded in the circuit simulator (pg. 300, abstract and "Summary of existing model).

Claim 91. A computer (inherent to SPICE platform pg. 300,abstract) readable storage device embodying a program of instructions executable by a computer (inherent to SPICE platform pg. 300,abstract) to perform the method of any one of claims 1 and 93-98.

Claim 92. A method for transmitting a program of instructions executable by a computer (inherent to SPICE platform pg. 300,abstract) to perform a process of simulating the degradation (pg. 300, Introduction) of a circuit, said method comprising: causing the transmission to a client device a program of instructions, thereby enabling the client device to perform, by means of such program, the process of the method of any one of claims 1, and 93-98.

Claim 93. The method of claim 1, wherein the circuit includes a plurality of distinct sets of components, the method further comprising: supplying an independent performance criterion for each set of said plurality of distinct sets of components from each of said sets of components, wherein each of the selected components' relative degradation (pg. 300, Introduction) parameter is determined using the respective performance criteria of the set to which the selected component belongs, and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with each of the specified components using eh respective aging model information and respective relative component degradation (pg. 300, Introduction) parameter at the supplied circuit stress (pg. 300, right column lines 10-11) time values.

Claim 94. The method of claim 1, wherein said supplying aging model information includes supplying aging model information on a first set of selected components of the circuit and wherein said simulating the behavior of the fresh circuit includes simulating the behavior of the fresh circuit to determine for each of the first selected set of components a component degradation (pg. 300, Introduction) parameter relative to circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph), the method further comprising: specifying the degradation (pg. 300, Introduction) level of a second set of selected components of the circuit, wherein the elements of the first set and the second set of components are distinct, and wherein said determining the degraded operation of the circuit includes determining the

degraded operation of the circuit by simulating the operation of the circuit by simulating the operation of the circuit with each of the first set of specified components using the respective aging model information and respective relative component degradation (pg. 300, Introduction) parameter at the supplied circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) values and with each of the second set of specified components using the respective specified degradation (pg. 300, Introduction) level.

Claim 95. The method of claim 1, further comprising: revising the netlist (inherent to SPICE program, pg. 300, Introduction), wherein each of said selected components is replaced by a on-aged version of the selected components and a plurality of independent current sources (pg. 302, right column, Evaluating Degradation Model Precision) corresponding to different mechanisms connected between the terminals of the non-aged version, wherein the magnitude of the current relative to a circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) in each of the current sources (pg. 302, right column, Evaluating Degradation Model Precision) of a component is determined from the aging model information of the component and a distinct mechanism degradation (pg. 300, Introduction) parameter derived from the component degradation (pg. 300, Introduction) parameter; and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist

(inherent to SPICE program, pg. 300, Introduction) at the supplied circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) values.

Claim 96. The method of claim 95, wherein said simulating the behavior is performed using a circuit simulator (pg. 300, abstract and "Summary of existing model) and includes incorporating the aging of the selected components by updating the models of said circuit simulator (pg. 300, abstract and "Summary of existing model).

Claim 97. The method of claim 1, wherein said simulating the behavior is performed using a circuit simulator (pg. 300, abstract and "Summary of existing model) and includes incorporating the aging of the selected components by updating the models of said circuit simulator (pg. 300, abstract and "Summary of existing model), and wherein said determining the degraded operation of the circuit at the supplied stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph) values by simulating the operation of the circuit with the each of the specified components using the respective aging model information and respective component degradation (pg. 300, Introduction) parameter at the supplied stress (pg. 300, right column lines 10-11) time values (pg. 305, right column, 2nd paragraph).

Claim 98. . The method of claim 1, wherein degradation (pg. 300, Introduction) parameter is a degradation (pg. 300, Introduction) level relative to circuit stress (pg. 300, right column lines 10-11) time (pg. 305, right column, 2nd paragraph), the method

further comprising: quantizing each of said relative degradation (pg. 300, Introduction) levels to one of a plurality of discrete values, and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the specified components using their respective aging model information and respective quantized relative degradation (pg. 300, Introduction) level at the supplied circuit stress (pg. 300, right column lines 10-11) time value (pg. 305, right column, 2nd paragraph).

Citation of Relevant Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

- Le et al., "Digital Test Circuit and Optimization for AC Hot-Carrier Reliability Characterization and Model Calibration under Realistic High Frequency Stress Conditions" IEEE 1997. pg. 56-62.

- Takeda-E., An Empirical Model for Device Degradation Due to Hot-Carrier Injection" IEEE 1983. pg. 111-113.

- Wu et al., "GLACIER: A Hot Carrier Gate Level Circuit Characterization Simulation System for VLSI Design" 2000 March. IEEE pg. 73-79.

- Aur et al., "Circuit Hot Electron Effect Simulation" 1987 Texas Instrument. pg. 498-501.

- Kim et al., "Oxide-Field Dependence of the NMOS Hot-Carrier Degradation Rate and Its Impact an AC-Lifetime Prediction". IEEE 1995. pg. 37-40.

- Chen et al., "Statistical Variation of NMOSFET Hot Carrier Lifetime and its Impact on Digital Circuit Reliability" IEEE. pg.29-32. 1995.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Should the applicant(s) have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

October 20, 2005

Paul L. Rodriguez 10/28/05
Primary Examiner
Art Unit 2125

TS